In the Claims

The following Listing of Claims replaces all prior versions in the application:

LISTING OF CLAIMS

1. (Currently Amended) Self aligned MIS transistor having in a substrate a source zone and a drain zone on either side of a channel zone, said source and drain zones comprising a buried zone in the substrate and a raised zone stacked on the buried zone, as well as a T shaped gate structure comprising:

a vertical bar located above the channel zone, surmounted by a horizontal bar extending on either side of the vertical bar, said horizontal bar having a lower part, a lateral part and an upper part, the gate structure comprising a stacking of one or several conductive layers, the gate structure having a base zone ~~at~~ around a base of the vertical bar~~, said base zone extending laterally beyond the base of the vertical bar of the T~~,

wherein the gate structure is coated with a shaping material, said shaping material covering the vertical bar of the T, the lower and lateral parts of the horizontal bar of the T, and the base zone said shaping material covering the base zone without extending laterally beyond a vertical projection, on the base zone, of the lateral part of the horizontal bar covered with the shaping material, said base zone covered by the shaping material covering at least a part of the buried zone of the source and drain zones and not the raised zone of the source and drain zones.~~of the gate structure including portions thereof extending laterally beyond the base of the vertical bar of the T, said base zone covered by the shaping material covering at least a part of the buried zone of the source and drain zones and not the raised zone of the source and drain zones.~~

2. (Canceled)

3. (Previously presented) Self aligned MIS transistor according to claim 1, further comprising first extension zones located between the channel and source and drain zones respectively and having a doping of the same nature as the sources and drain zones but weaker.

4. (Previously presented) Self aligned MIS transistor according to claim 1, further comprising second extension zones located between the channel and source and drain zones respectively and having a doping of nature opposite to that of the source and drain zones.

5. (Previously presented) Self aligned MIS transistor according to claim 3, characterised in that the second extension zones between the first extension zones and the channel zone have respectively a doping of nature opposite to that of the source and drain zones.

6. (Previously presented) Self aligned MIS transistor according to claim 1, characterised in that the shaping material is of silicon nitride (Si_3N_4) or hafnium oxide (HfO_2) or zirconium oxide (ZrO_2) or aluminum oxide (Al_2O_3).

7. (Previously presented) Self aligned MIS transistor according to claim 1, characterised in that the stacking of layers constituting the gate structure lodged in the shaping material is intrinsic polysilicon or metal.

8. (Currently Amended) Method for manufacturing, on a semiconductor substrate, at least one self aligned MIS transistor having a source zone and a drain zone on either side of a channel zone, said source and drain zones comprising a buried zone in the substrate and a raised zone stacked on the buried zone, as well as a T shaped gate structure of low resistivity comprising a vertical bar located above the channel zone, surmounted by a horizontal bar extending on either side of the vertical bar, said horizontal bar having a lower part, a lateral part and an upper part, the gate structure comprising a stacking of one or several conductive layers, the gate structure having a base zone ~~at~~around a base of the vertical bar, ~~said base zone extending around the base of the vertical bar of the T,~~ the method comprising a step of forming a solid shape having the T shape of the gate ~~that one wishes to form~~to be formed, and the coating of said shape in a shaping material, said shaping material coating the lateral surface of the vertical bar of the T, and the lower and lateral surfaces of the horizontal bar of the T,

wherein said shaping material also covers the base zone without extending laterally beyond a vertical projection, on the base zone, of the lateral part of the horizontal bar covered with the shaping material and at least a part of the buried zone of the source and drain zones and does not cover the raised zone of the source and drain zones.~~of the gate structure and at least a~~

~~part of the buried zone of the source and drain zones and does not cover the raised zone of the source and drain zones.~~

9. (Canceled)

10. (Original) Method according to claim 8 characterised in that the shaping material is silicon nitride (Si_3N_4) or hafnium oxide (HfO_2) or zirconium oxide (ZrO_2) or aluminum oxide (Al_2O_3).